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BI-DIRECTIONAL BUS BRIDGE IN WHICH MULTIPLE DEVICES CAN ASSERT BUS CONCURRENTLY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] Not applicable.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] Not applicable.

BACKGROUND OF THE INVENTION

<u>Field of the Invention</u>

[0003] The present invention generally relates to a bus bridge. More particularly, the invention relates to a bi-directional bridge for use with buses in which multiple devices may attempt to drive the bus concurrently. More particularly still, the invention relates to an I^2C bus bridge.

<u>Background of the Invention</u>

[0004] Modern computer systems generally include a plurality of devices interconnected through a system of buses. For example, a conventional computer system typically contains one or more central processing unit (CPUs) coupled through a host bridge to a main memory unit. A CPU bus usually couples the CPU(s) to the host bridge, and a memory bus connects the bridge to the main memory. The host bridge typically includes a memory controller which receives memory access requests (such as from the CPUs) and responds by generating standard control signals necessary to access the main memory.

[0005] Other types of buses may also be present in a computer system. The I^2C bus developed by Philips is one such example. The I^2C bus generally has a simple architecture, is easy to use and is thus becoming widely used. The I^2C bus has one or more characteristics that may also be found in other buses now known or later developed. One such characteristic is that only a limited number of devices can be connected to any one bus. This limitation results from electrical loading and noise concerns. Accordingly, if the number of I^2C-compliant devices desired to be included in a system increases, a system designer is forced to include more than one I^2C bus in the system. It is not uncommon today for a system to have multiple I^2C buses with each bus having one or more devices connected thereto.

[0006] It may be desired for a device attached to one I^2C bus to communicate with a device attached to another I^2C bus. One way to permit this communication, albeit in a less than efficient manner, includes using the core logic of the system (*e.g.*, the host processor) to pass information from one I^2C bus to another. Another technique would be to bridge the two I^2C buses together.

[0007] The bridge solution is not simple and straightforward because of another characteristic of the I^2C bus in which more than one device attached to the bus may attempt to drive the bus at a time. Concurrent bus assertion is common during the I^2C bus arbitration process, for example. Also, slave devices may attempt to drive a bus while a master is driving the bus in order to cause the transaction to stall for one reason or another. When a device drives the bus, the device typically pulls one of the bus signals low. Another device may drive that same signal low. Because a second device is driving the signal low, the signal will remain low even if the first device releases the signal. This is generally true because of the open-collector or open-drain nature of the I^2C bus. This characteristic makes it difficult to bridge two I^2C buses together.

[0008] An example will help clarify the problem. A bridge may couple together two I^2C buses (designated A and B). If a master on bus A drives the clock signal low, the bridge should detect that event and drive the corresponding clock signal low on B bus. If, while the B bus clock signal is low, a device on the B bus attempts to force low that already low clock signal, the bridge will not be able to detect this occurrence because the clock signal is already low. Then, if the master on bus A that initially drove the clock signal low releases its hold of the clock signal and the bus B device is still driving bus B's clock signal low, the bridge will not know to keep the bus A clock signal low.

[0009] A solution to this problem is needed. Such a solution preferably should be inexpensive to implement.

BRIEF SUMMARY OF THE INVENTION

[0010] The problems noted above are solved in large part by a bridge device, particularly useful in computer systems, which can detect whether the same signal on two separate buses is being actively asserted by devices on both buses. The bridge preferably includes comparators to drive or assert signals on one bus only if the signal is being asserted by the corresponding signal on the other of said buses. That is, the bridge does not drive a signal on a bus that is already being actively driven by a device coupled to that very bus if the same signal is not being driven by a device on another bus connected to the bridge.

[0011] By way of example, if a device coupled to a first bus asserts a signal (*e.g.*, low), a comparator in the bridge detects this condition and causes the corresponding signal on the second bus to be asserted. The bridge, however, does not attempt to drive the same signal on the first bus that is already being asserted. This is particularly useful in a bi-directional bus in which one or more signals can be asserted concurrently by more than one device on the bus. If devices on both

buses concurrently assert the same signal to the same logic level, the bridge detects this condition. Then, if one of the devices attempts to release the signal, the bridge will continue to assert that signal on that same bus, even though the signal was released by the device on that bus, because the device on the other bus is continuing to assert the same signal.

[0012] The preferred embodiment of the bridge includes a comparator corresponding to each bus signal and for each bus. Thus, if each bus (*e.g.*, an I^2C bus) has two signals, the bridge will have four comparators—two comparators for the two signals on one bus and another pair of comparators for the corresponding two signals on the other bus. Each comparator has two inputs. One input is coupled to a threshold voltage and the other input is coupled to a bus signal from both buses. The bus signal input to the comparator will be at a voltage level that will differ depending on which bus is actively driving the signal. A resistor included in the circuit ensures that two different voltage levels will occur depending on the source of the signal. The threshold input is set at a voltage level that is between these two voltage levels of the bus signal input. Accordingly, the comparator is able to determine which bus is actively driving the signal and then only drive the bus signal on the bus to which the comparator's output is coupled if the bus signal is being actively driven by the other bus.

[0013] This type of bus bridge is elegantly simple and straightforward and works well for buses in which a signal can be concurrently asserted by more than one device. Further, the bridge can be used to bridge together two buses operating from different power planes, while maintaining each bus electrically isolated from the other bus. These and other advantages will become apparent upon reviewing the following disclosures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] For a detailed description of the preferred embodiments of the invention, reference will now be made to the accompanying drawings in which:

[0015] Figure 1 shows a computer system embodying the preferred embodiment of the invention in which an I^2C bus bridge is included;

[0016] Figure 2 conceptually illustrates how the bus bridge can distinguish between an external device asserting a signal or the bridge itself asserting the signal;

[0017] Figure 3 shows a schematic of a comparator used in the bridge; and

[0018] Figure 4 shows a complete schematic of an I^2C-to- I^2C bus bridge in accordance with the preferred embodiment of the invention.

NOTATION AND NOMENCLATURE

[0019] Certain terms are used throughout the following description and claims to refer to particular system components. As one skilled in the art will appreciate, computer companies may refer to a component and sub-components by different names. This document does not intend to distinguish between components that differ in name but not function. In the following discussion and in the claims, the terms "including" and "comprising" are used in an open-ended fashion, and thus should be interpreted to mean "including, but not limited to...". Also, the term "couple" or "couples" is intended to mean either a direct or indirect electrical connection. Thus, if a first device couples to a second device, that connection may be through a direct electrical connection, or through an indirect electrical connection via other devices and connections. In addition, no distinction is made between a "processor," "microprocessor," "microcontroller," or "central processing unit" (CPU) for purposes of this disclosure. To the extent that any term is not specially

defined in this specification, the intent is that the term is to be given its plain and ordinary meaning.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] The preferred embodiment described below is shown in the context of a bridge for coupling together two I^2C buses. Broadly, however, this disclosure and the claims which follow should not be limited to just the I^2C bus, but rather should apply to bridging other types of buses.

[0021] Referring now to Figure 1, system 100 is shown constructed in accordance with a preferred embodiment of the invention. As shown, system 100 includes one or more host processors 102, a host bridge 110, system memory 120, a south bridge 130, an input device 132, and various devices 136, 146 attached to I^2C buses 138 and 148 coupled together by I^2C bridge 140. The host bridge 110 couples to the processors 102, memory 120 and the south bridge 130. The bus 125 (which may be a high speed serial link such as those links proprietary to Intel and ServerWorks or a peripheral component interconnect bus) interconnecting the north and south bridges 110, 130 may have one or more devices such as modems, network interface cards (NICs), and the like attached thereto (none shown in Figure 1).

[0022] As shown, the south bridge 130 preferably includes an I^2C bus master slave 136 for permitting south bridge 130 to couple to the I^2C bus 138 to which one or more devices 136 are attached. Such devices can be any desired I^2C bus-compliant device. Further, although the I^2C bus 138 is shown coupled to the south bridge 130, the bus need not be coupled to south bridge 130. For example, the I^2C bus 138 may be coupled to the host bridge 110 or other devices in the system. Further, other system architectures besides that shown in Figure 1 are possible also; the architecture in Figure 1 is merely exemplary of one suitable embodiment. The salient feature of this disclosure is the bridging together of two I^2C buses.

[0023] The I^2C bus bridge 140 shown in Figure 1 bridges together the two buses 138 and 148 as shown. For the purpose of explaining the function of the bridge, the bus 138 is referred to as the "A" bus, while the bus 148 is referred to as the "B" bus. Bridge 140 permits a device on the A bus to communicate with a device on the B bus. The communication pathway is bi-directional. That is, a bus A device can become a master in which the target slave device is on the B bus, and vice versa.

[0024] In accordance with the preferred embodiment, the bridge 140 detects when a device connected to the A bus asserts one of the bus signals and then drives the corresponding signal on the B bus. Then, if a device on the B bus drives that same signal, the bridge 140 detects this event and responds by driving that same signal on the A bus, even after the original bus A device releases the signal. In other words, the bridge 140 is able to determine which or both sides of the bridge is driving a particular signal.

[0025] This concept is illustrated in Figure 2. The bridge 140 is shown conceptually in Figure 2 as containing two comparator circuits 142, one for each side (A and B) of the bridge. Each comparator 142 compares the voltage level of a bus signal from the devices attached to one bus to a reference voltage (labeled as "threshold" in Figure 2). As such, the signals on the A bus are compared to a threshold as are the signals on the B bus. The comparators are "cross coupled" as shown meaning that the output signal of each comparator is coupled to an input of the other comparator and, in fact, coupled to a signal from the other bus. Tracing the schematic from the perspective of the A side of the bridge, the devices 136 are wired together and to an input of the A comparator 142. The output of the B comparator is also connected to A comparator's input and to the A bus signal(s). The threshold level of the A comparator is set so that if either device 136 actively asserts a signal (*e.g.*, drives the signal low), the output signal from the A comparator will

be similarly asserted (*i.e.*, driven low), thereby asserting the corresponding signal on the B side of the bridge. If, however, none of the A devices 136 drive the signal low, the signal will remain high and the output of the A comparator will be high on the B side of the bus as well.

[0026] Referring still to Figure 2, if a device 146 on the B side of the bridge drives the signal low when an A device 136 is already driving its corresponding signal low as noted above (*i.e.*, devices on opposite sides of the bridge are driving the same signal low), both comparators 142 will drive their output signals low. The A comparator will drive its output low because one of the A devices is driving the signal low. Similarly, the B comparator, which is coupled to the same signal, will drive its output low because one of the B devices is driving its signal low. Thus, if the A device releases its signal permitting it to become high, the B comparator, which is coupled to the same signal, will keep that signal low because a B device is actively driving the signal low on the B side of the bridge.

[0027] As shown in the configuration in Figure 2, all device 136, 146 are coupled to the inputs of both comparators. The devices 136 on the A side of the bridge are wired directly to the A comparator as shown. The devices 146 on the B side of the bridge are also coupled to the A comparator, albeit via the B comparator. Preferably, the bridge 140 is able to determine which side of the bus is driving a bus signal, or whether devices on both sides of the bus are actively driving the signal. To this end, the bridge 140 is designed so that a different voltage level is generated on the input of a comparator depending on whether a bus device connected to that input asserts the signal or whether the signal is being asserted by a bus device on the other bus via the other comparator. For example, the voltage or input 143 of the A comparator will be at one level if a device 136 asserts the signal and at a second if a device 146 asserts the same signal. One embodiment in which this can be accomplished is shown in Figure 3, and will be discussed below.

The threshold level for both comparators is set at a level that can distinguish between these two voltage levels.

[0028] Referring now to Figure 3, an exemplary embodiment of at least a portion of a comparator circuit 142 which performs the function described above is shown. The circuit is shown to bridge a single bus signal 152 (*e.g.*, the I^2C bus clock signal SCL) between devices 136 on the A side of the bridge and the corresponding signal 154 (SCL) on the B side of the bridge. The comparator circuit includes a comparator 150 (*e.g.*, an LM339) and resistors R1-R7. Resistors R4 and R5 comprise a voltage-divider, the mid-point 145 of which represents the threshold voltage which is provided to the inverting input of the comparator 150. The A devices 136 couple to the non-inverting input of the comparator via resistor R3. When a device 136 pulls the SCL(A) signal 152 low, the voltage on the non-inverting input of the comparator 150 will become a voltage within a first voltage range which is less than the threshold value on the inverting input. The comparator 150 responds by forcing its output signal, SCL(B), low through a driver (not specifically shown). Once the SCL(A) signal is released to go high by device 136, the comparator 150 responds by releasing the SCL(B) signal to go high as well. In this manner, the clock signal from the A bus is bridged to the B bus.

[0029] The B comparator 142 (Figure 2) may attempt to drive the A side clock signal low as a result of a bus B device 146 actively forcing the clock signal low. As shown in Figure 3, the clock signal from the B comparator is also provided to the non-inverting input of the comparator 150 via resistors R7 and R3. Resistor R7 preferably is set at a value such that, when a B bus device drives the clock signal low, the resulting voltage on the non-inverting input of the comparator 150 will be higher than the threshold level, but still at a level that is recognized as a low value on the bus. Thus, when a device on the A side of the bridge pulls the clock signal low, the comparator's non-

inverting input will be pulled down to a level in a first voltage range. When a device on the B side of the bus pulls the clock signal low, the comparator's non-inverting input will be pulled down to a level in a second voltage range via the other comparator in the bridge. The threshold level set by voltage-divider R4 and R5 preferably is set between the first and second voltage ranges so that the comparator can distinguish the source of the low signal. Further, if devices on both sides of the bus actively pull the clock signal concurrently, the non-inverting input will be driven to a low level in the first voltage range so that the comparator 150 will drive the bus B clock low even if the bus B device releases the clock signal.

[0030] In accordance with one suitable embodiment of the invention, the resistors R1-R7 have the following values as listed in Table I.

Table I. Resistor Values

Resistor	**Value (ohms)**
R1	10K
R2	1M
R3	20K
R4	210K
R5	10K
R6	4.7K
R7	470

[0031] With the exemplary set of values shown in Table I and with a VCC of 3.3 V, the threshold voltage is approximately 150 mV. The devices 136 will be able to pull the SCL(A) down to a value of about 30-40 mV (the first voltage range). With a value of R7 of 470 ohms, the other comparator within the bridge will be able to pull the SCL(A) down to a value of about 300-340 mV (the second voltage range). Thus, the threshold voltage of 150 mV is between these two ranges and thereby permits the bridge to determine the source of a low bus signal.

[0032] As explained above, each comparator actively drives a signal on one of the busses only if a device on its input bus is actively driving that signal. There are three conditions that are

relevant to the operation of a comparator and each of these three conditions are addressed in the following table. The table examines the action of the comparator 142 from Figure 2 whose input is taken from the A side of the bridge (bus segment A) and whose output drives the B side of the bridge (bus segment B).

Table II. Comparator Action

Bus segment A state (comparator input)	**Comparator input voltage**	**Bridge action on segment B (comparator output)**
No bus A device is driving bus	300-340mV	Comparator does not drive bus B
Bus being driven only by a bus A device	30-40mV	Comparator does drive bus B
Bus being driven by a bus A device and a bus B device	30-40mV	Comparator does drive bus B

[0033] Referring now to Figure 4, a complete schematic of a bus bridge 140 in accordance with the preferred embodiment is shown. The bridge 140 comprises two comparator units 142a and 142b. Comparator unit 142a responds to signals being asserted on the A side of the bridge to drive the corresponding signal on the B side to appropriate levels. Similarly, comparator unit 142b responds to signals being asserted on the B side of the bridge to drive the corresponding signal on the A side to appropriate levels. Each comparator unit 142a, 142b preferably includes a comparator circuit as in Figure 3. If the buses being bridged together are I^2C buses which comprises two signals—a clock signal (SCL) and a data signal (SDA)—each comparator unit preferably includes two comparator circuits, one circuit for each signal.

[0034] If it is desired to turn the bridge function on and off, an enable feature can be included within the bridge. One suitable embodiment for such an enablement feature is represented by the OR gates 160 and enabling drivers 162. Each such driver 162 is enabled by its corresponding OR gate whose inputs are the output of a comparator 150 and an enable signal which can be asserted by a device or signal external to the bridge 140. The driver 162 will release the bus interface signal

(to float high) if the circuit is disabled (*i.e.*, the enable signal is high) or the output of the comparator reflects that a device on the other bus is no longer driving.

[0035] Besides bridging together two buses for the sake of permitting devices on two different buses to be able to communicate with each other, the bridge herein described provides another use. That use is to electrically isolate, as well as bridge together, two buses that operate from different power planes (*i.e.*, different voltage sources). One bus may operate from "auxiliary" power which is always on as long as the computer is connected AC power even if the computer is powered off. Another bus may be powered from a different source within the computer that is on only when the computer is powered on. In this situation—bussed operating from different power sources—the bridge 140 described above can be used, not only simply to bridge the buses together, but also to electrically isolate the buses. As shown in Figure 4, the power used to operate the comparators which drive the clock and data signals on the A bus is labeled as VCC while the power input to the other comparators which drive the B bus signals is labeled as VDD. By using two different power sources for VCC and VDD, the buses can be electrically isolated.

[0036] The above discussion is meant to be illustrative of the principles and various embodiments of the present invention. Although the active state of the I^2C bus signals described above is the logic low state, the principles discussed above may be adapted to apply to logic high active states as well. Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.